PNI Application Note:

3D MagIC & MagI2C MLF Land Pattern and SMT Assembly Guidelines

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1 Introduction

This application note provides printed circuit board (PCB) designers with guidelines for mounting PNI Sensor Corporation's 3D MagIC and MagI2C ASICs packaged in Amkor's MicroLeadFrame® package. The MicroLeadFrame package (MLF) is an encapsulated package with a copper lead frame substrate. Electrical contact to the PCB is made by soldering the lands on the bottom surface of the package to the PCB. The exposed die-attach paddle on the bottom of the MLF efficiently conducts heat to the PCB, which helps stabilize the ASIC temperature.

Note: This document serves as a guideline to help the user develop a proper PCB design and surface mount process. Actual studies and other development effort may be needed to optimize the process to the user's surface mount requirements.

Figure 1: Punch-Singulated MLF Section Drawing

2 Considerations for Mounting MLF Package

For optimal performance, special consideration should be followed in designing the user's PCB and mounting the package. For enhanced thermal, electrical, and board-level performance, the exposed paddle on the package needs to be soldered to the PCB using a corresponding thermal pad on the PCB. Additionally, the PCB design needs to take into consideration dimensional tolerances imposed by the MLF package, PCB, and assembly.

A number of factors affect mounting of the MLF package to the PCB, including: the solder paste coverage in the thermal pad region, the stencil design for the peripheral and thermal pad region, the stencil thickness, the lead finish on the package, the surface finish on the PCB, the type of solder paste, and the reflow profile. This application note covers these issues.

3 PCB Design Guidelines

As shown in Figure 2 and Figure 3, the lands on the bottom of the MLF are rectangular with rounded corners on the inside. Since the MLF does incorporate solder balls, the electrical connection between the ASIC and a PCB is made by printing the solder paste on the PCB and reflowing it after placing the ASIC. In order to form reliable solder joints, special attention is needed in designing the PCB pad pattern and solder paste mask.

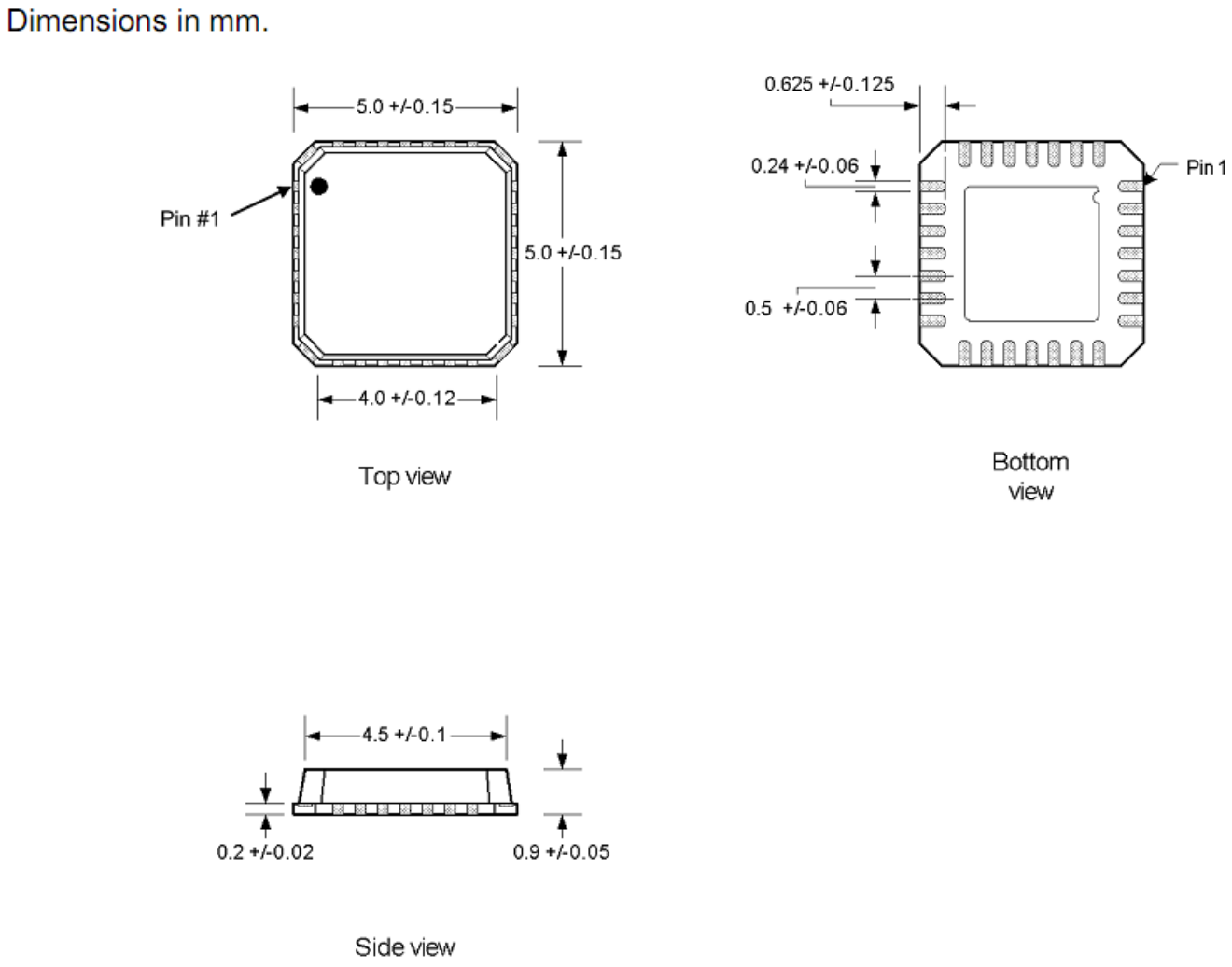


Figure 2: 3D MagIC MLF package dimension

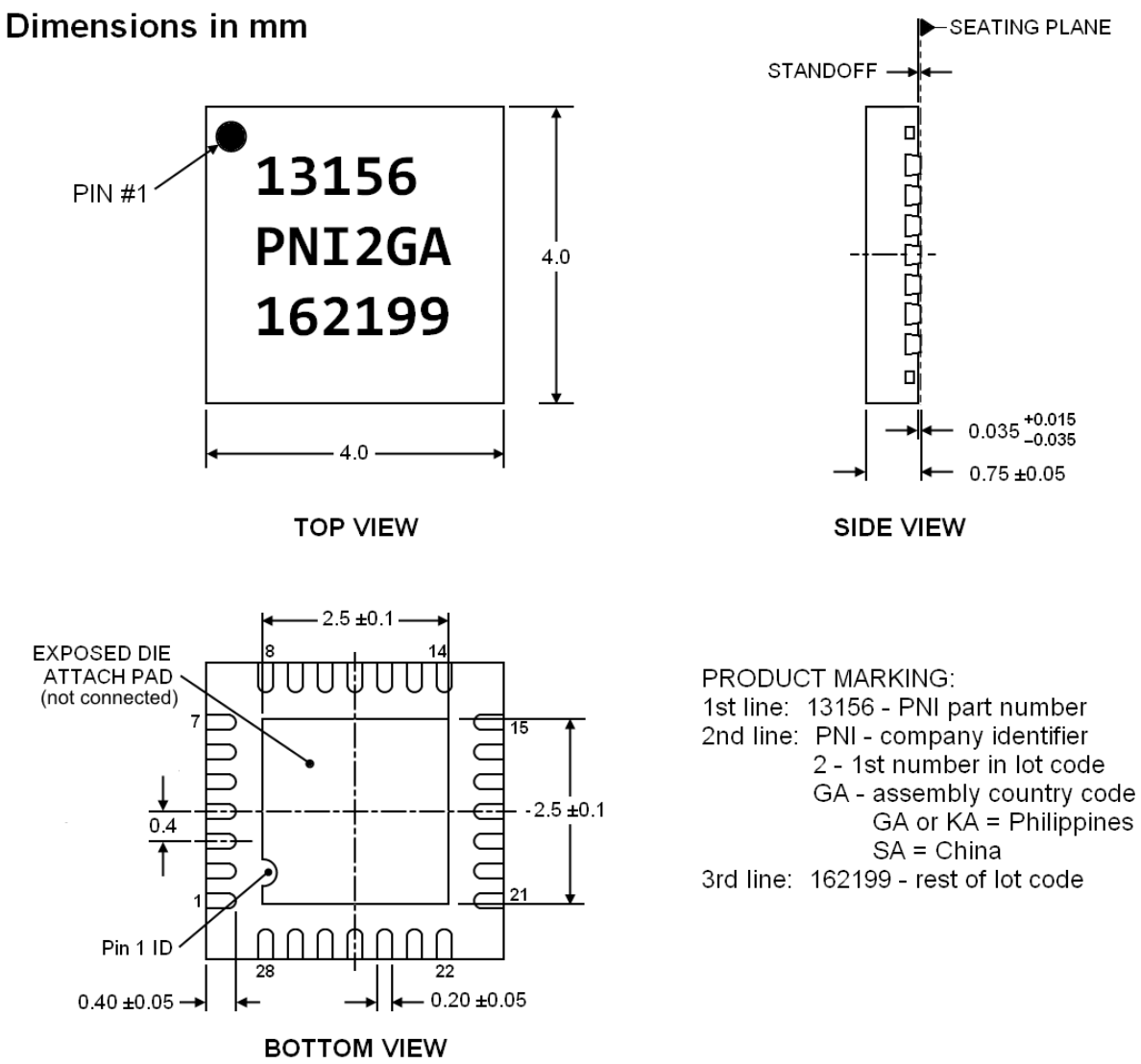


Figure 3: MagI2C MLF package dimension

3.1 Perimeter Pads Design

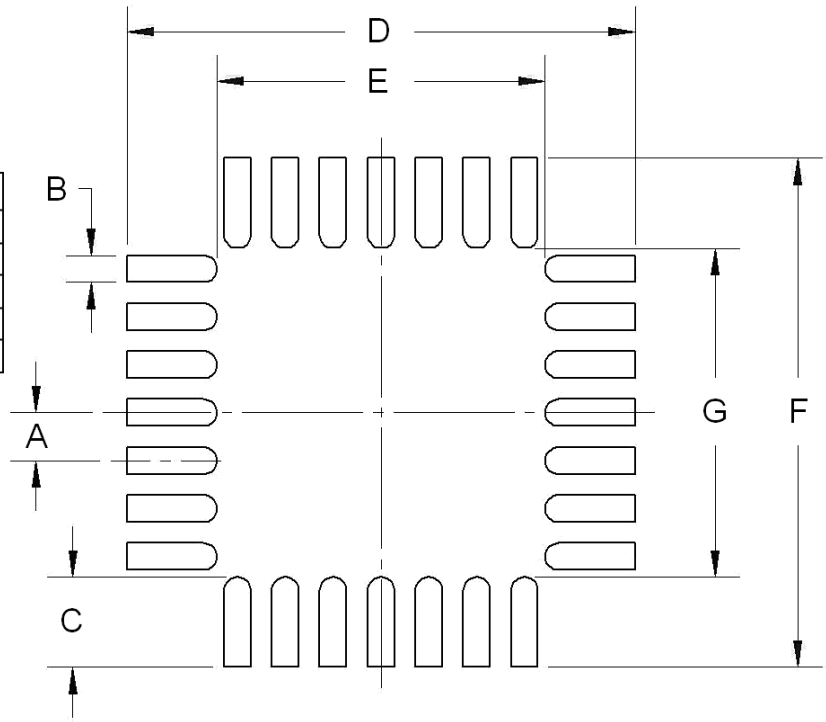
Typically the PCB pad pattern is based on guidelines developed within a company or by following industry standards such as IPC-SM-782. For the purpose of this document, IPC's methodology is used for designing the PCB pad pattern. However, due to the exposed die paddle and the package lands on the bottom side of the package, certain constraints are added to IPC's methodology. The pad pattern developed here includes considerations for lead and package tolerances.

3.2 PCB Pad Pattern

The recommended PCB land pattern for mounting the 3D MagIC MLF and MagI2C are given in Figure 4.

Dimensions in mm

	3D MagIC	MagI2C
A	0.50 typ.	0.40 typ.
B	0.28 max.	0.20 max.
C	0.94 typ.	0.60 typ.
D, F	5.30 typ.	4.80 typ.
E, G	3.43 min.	3.00 min.



PCB LAND PATTERN

Figure 4: 3D MagIC PCB Land Pattern

3.3 Thermal Pad Design

The MLF package is designed to provide superior thermal performance. This is partly achieved by incorporating an exposed die paddle on the bottom surface of the package. To take full advantage of this feature, the PCB must have features to effectively conduct heat away from the package. This typically is achieved by incorporating a thermal pad and thermal vias on the PCB. Since PNI's 3D MagIC and MagI2C ASICs are low-power-consumption devices, thermal vias provide little benefit and incorporating them potentially introduces new failure mechanisms. For this reason ***PNI recommends NOT soldering to the thermal die paddle.***

3.4 Solder Masking Considerations

Sample solder mask patterns for the 3D MagIC and MagI2C are given below in Figure 5 and Figure 6.

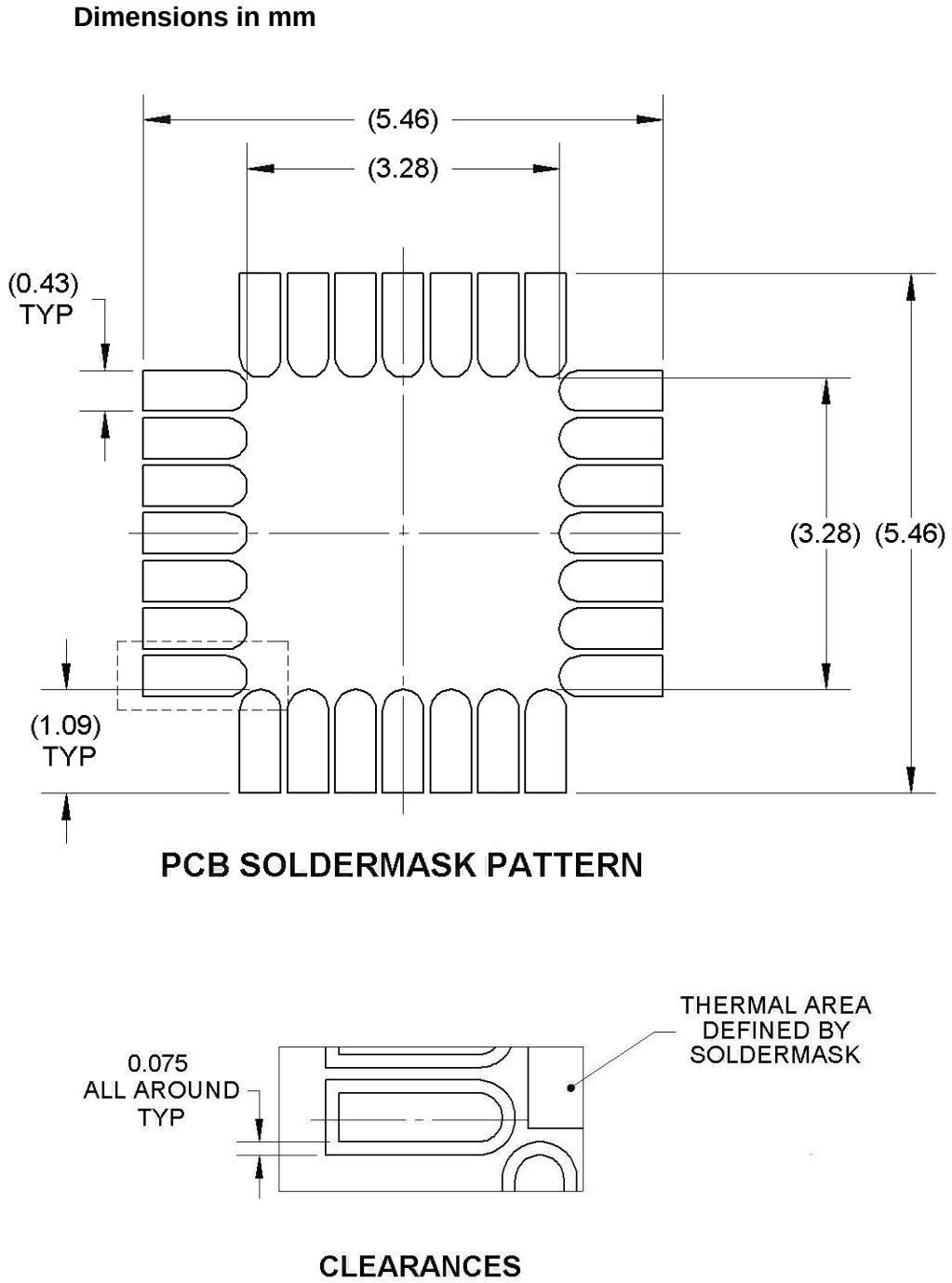


Figure 5: Typical 3D MagIC PCB Solder Mask Pattern

Dimensions in mm

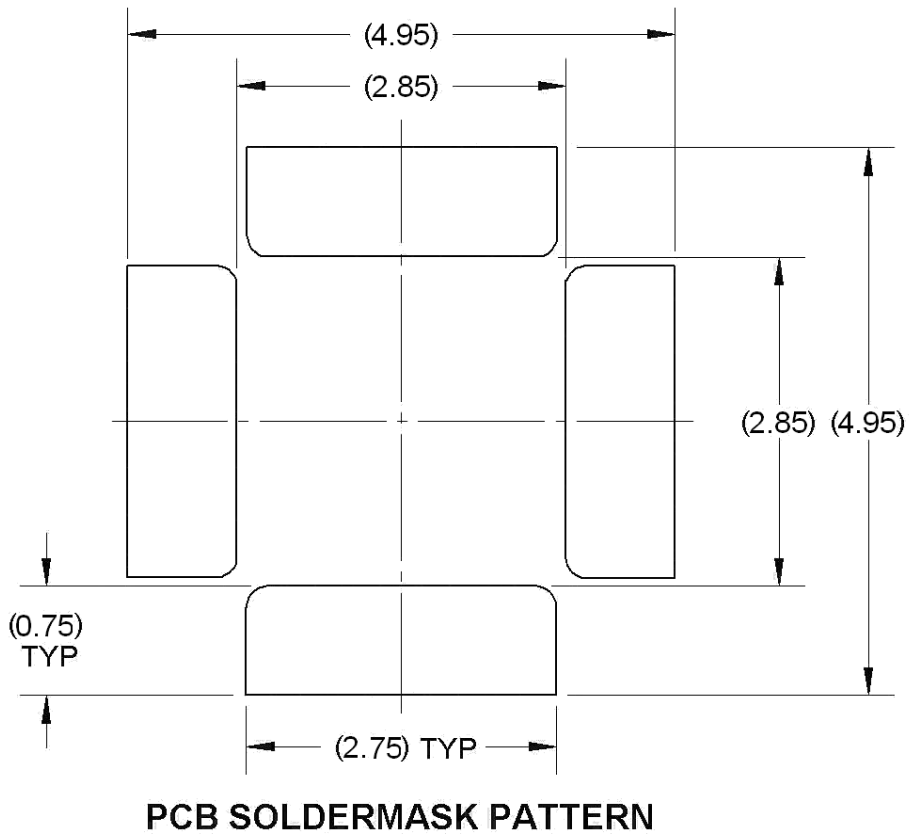


Figure 6: Typical MagI2C PCB Solder Mask Pattern

The landing pads on the PCB can be either solder-mask defined (SMD) or non-solder-mask defined (NSMD). Using copper to define the land pattern (NSMD process) provides greater precision that using a solder mask to define the pattern (SMD process). Also, an NSMD pad with a solder mask opening larger than the metal pad will provide a more reliable solder joint than an SMD pad since solder is allowed to wrap around the sides of the metal pad. Because of this, NSMD pads are recommended over SMD pads.

The solder mask opening should be 120 to 150 µm larger than the pad, resulting in a 60 to 75 µm clearance between the copper pad and the solder mask. This accommodates the solder mask registration tolerances, which usually are 50 to 65 µm, depending on the PCB fabricator's capabilities. Typically each pad on the PCB should have its own solder mask opening with a web of solder mask between two adjacent pads. Since the web has to be at least 75 µm wide for the solder mask to stick to the PCB surface, each pad can have its own solder mask opening for lead pitches of ≥0.5 mm. For ≤0.4 mm pitch parts with PCB pad

widths of 0.25 mm, not enough space is available for a solder mask web between the pads. In such cases, a "trench" type solder mask opening is recommended, wherein an opening is designed around all pads on each side of the package with no mask webbing between the pads, as shown in Figure 7. Note that the inner edge of the solder mask should be rounded, especially for corner leads, to allow sufficient solder mask webbing in the corner areas.

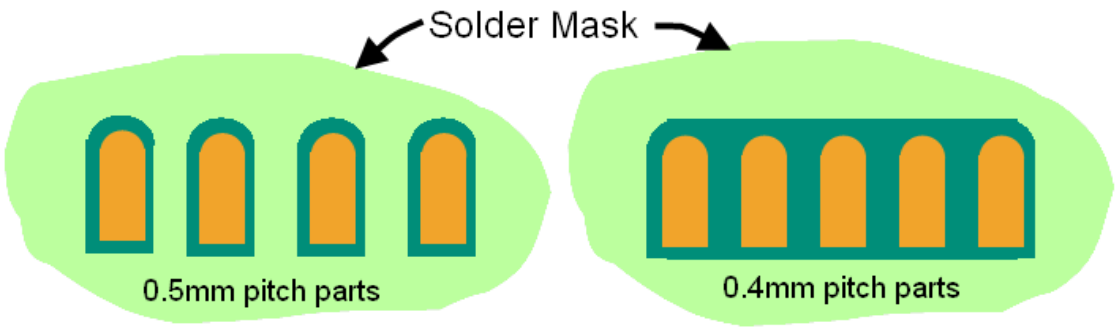


Figure 7: Illustration of Solder Mask Web

When the thermal land pad dimension is close to the theoretical maximum discussed above, it is recommended the thermal pad area be solder-mask defined (SMD) to avoid solder bridging between the thermal pad and the perimeter pads. The mask opening should be 100 µm smaller than the thermal land size on all four sides. This will ensure a 25 µm solder mask overlap even for the worse case misregistration.

4 PCB Mounting Guidelines

Because of the MLF's small lead surface area and sole reliance on printed solder paste on the PCB surface, forming a reliable solder joints takes special care. This is further complicated by the large thermal pad under the package and its proximity to the inner edges of the leads. Although the pad pattern designs suggested above help eliminate some surface mounting issues, special consideration is needed in stencil design and paste printing for both the perimeter and thermal pads. Since surface mount processes vary from company to company, careful process development is recommended. The following provides guidelines for a stencil design based on Amkor's experience in surface mounting MLF packages.

4.1 Solder Paste Stencil Design for Perimeter Pads

Solder joints on the perimeter pads should have a 50 to 75 µm standoff height and a good side fillet on the outside. A joint with a good standoff height but no or low fillet will have reduced life but may meet application requirements. The first step in achieving good standoff is ensuring a good solder paste stencil design for the perimeter pads. The stencil

aperture opening should be designed so maximum paste release is achieved. This usually is accomplished by considering the following two ratios:

- Area Ratio = Area of Aperture Opening/Aperture Wall Area, and
- Aspect Ratio = Aperture width/ Stencil Thickness

For rectangular aperture openings, as required for this package, these ratios are given as

- Area Ratio = LW/2T(L+W), and
- Aspect Ratio = W/T

Where L and W are the aperture length and width, and T is stencil thickness. For optimum paste release, the area and aspect ratios should be greater than 0.66 and 1.5 respectively.

It is recommended the stencil aperture be a 1:1 match with the PCB pads since both the area and aspect ratio targets are achieved easily with such an aperture. The stencil openings can be reduced for lead pullback because the pad on the package is smaller than the PCB pad. The stencil should be laser cut and electro polished. The polishing process smooths the stencil walls for improved paste release. Also, the stencil aperture tolerances should be tightly controlled, especially for 0.4 and 0.5 mm pitch devices, as these tolerances can effectively reduce the aperture size.

4.2 Stencil Design for Thermal Pad

As previously mentioned in Section 3.3, the MFL incorporates a thermal die pad to assist in heat flow, but PNI's ASICs are low-power-consumption devices and do not benefit from this feature. Indeed, since incorporating thermal vias to access the die pad potentially introduces new failure mechanisms, ***PNI recommends NOT soldering to the thermal die paddle.***

4.3 Stencil Thickness and Solder Paste

A stencil thickness of 0.125 mm is recommended for 0.4 and 0.5 mm pitch parts and can be increased to 0.15 to 0.2 mm for coarser pitch parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

"No Clean", Type 3 paste is recommended for mounting MLF packages, specifically because insufficient space is available under the part after reflow. A nitrogen purge also is recommended during reflow.

4.4 Reflow Profile

The reflow profile and peak temperature has a strong influence on void formation. Amkor has conducted experiments with different reflow profiles (ramp-to-peak vs. ramp-hold-ramp), peak reflow temperature, and time above liquids using Alpha Metal's UP78 solder paste (63% Tin / 37% Lead). Some representative profiles are shown in Figure 8.

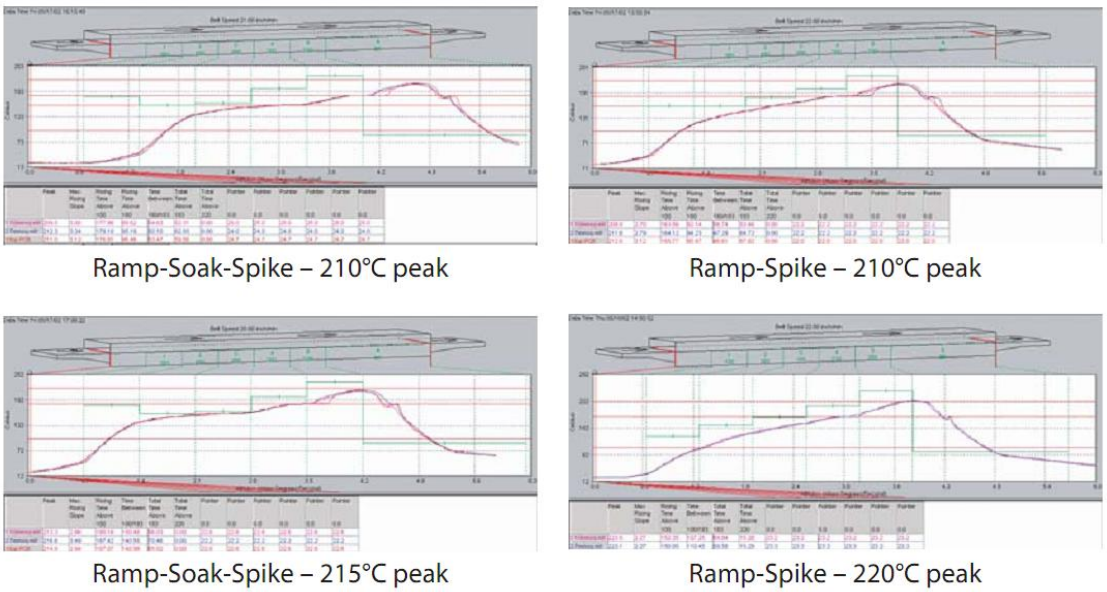


Figure 8: Various Reflow Profiles

4.5 Lead-free solder

For lead-free soldering of the PNI's MLF ASICs, PNI recommends the reflow profile given in Figure 9 and Table 1.

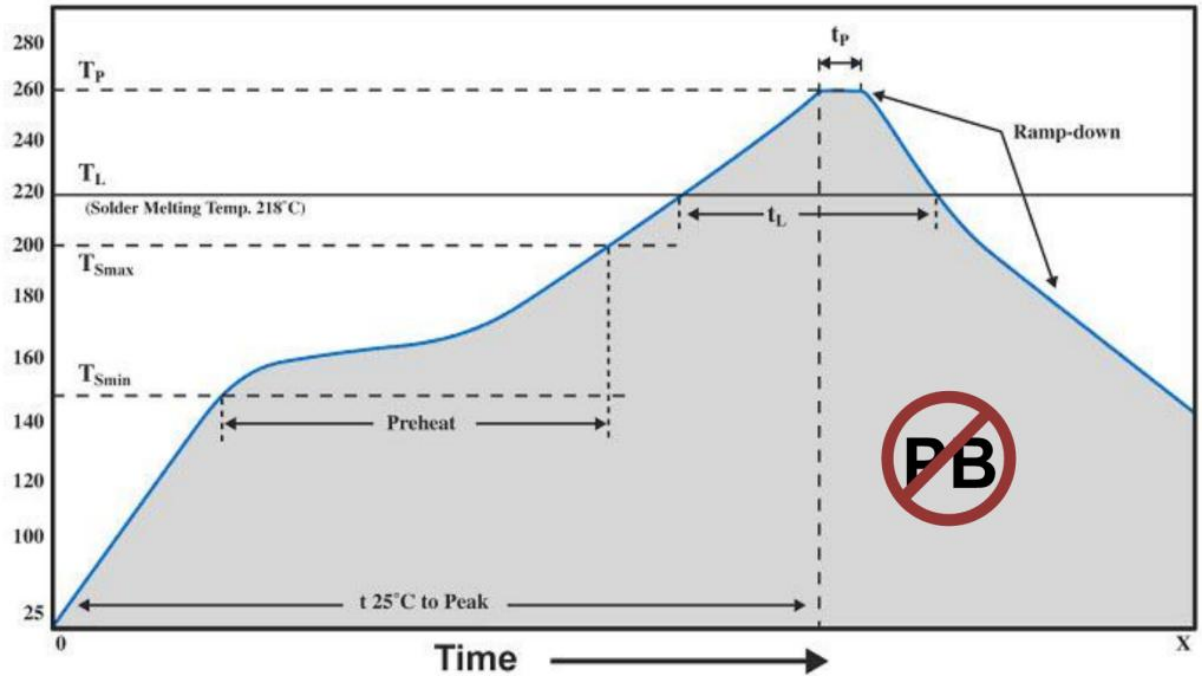


Figure 9: Lead Free Reflow Profile

Table 1: Recommended Process Parameters

Parameter	Symbol	Value
Preheat Temperature, Minimum	T_{Smin}	150°C
Preheat Temperature, Maximum	T_{Smax}	200°C
Preheat Time (T_{Smin} to T_{Smax})		60-180 Seconds
Solder Melt Temperature	T_L	>218°C
Ramp-Up Rate (T_{Smax} to T_L)		3°C/second max
Peak Temperature	T_P	<260°C
Time from 25°C to Peak (T_P)		6 minutes max
Time Above T_L	t_L	60-120 seconds
Soak Time (within 5°C of T_P)	t_P	10-20 seconds
Rampdown Rate		4°C/second max

Note: Meets lead-free profile recommendations (IPC/JEDEC J-STD-020)

5 Assembly Process Flow

Figure 10 shows the typical process flow for mounting the MLF to a PCB. It is important to include post-print and post-reflow inspection, especially during process development. The volume of paste deposited should be measured either by 2D or 3D techniques. If the paste volume is 80% to 90% of the stencil aperture volume, this indicates good paste release. After reflow, the mounted package should be inspected in a transmission x-ray for the presence of voids, solder balling, or other defects. Cross-sectioning also may be required to determine the fillet shape and size and joint standoff height.

With regard to leaded solder; typical reflow profiles for No Clean solder leaded paste are shown in Figure 8. Since the actual reflow profile depends on the solder paste being used and the board density, PNI does not recommend a specific profile for leaded solder. Note that the temperature should not exceed the MLF's maximum rated temperature for the given moisture sensitivity level. The time above liquidus temperature should be around 60 seconds and the ramp rate during preheat should be 3°C/second or lower.

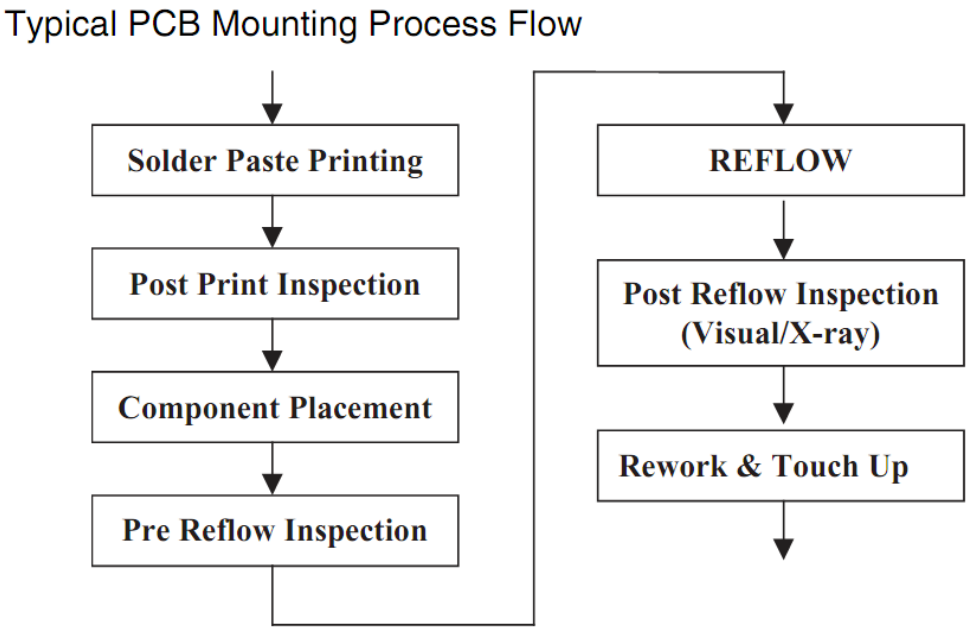


Figure 10: Typical PCB mounting process flow

6 Rework Guidelines

Since solder joints are not fully exposed in the case of MLFs, retouch is limited to the side fillet. For defects under the package, the whole package must be removed. Rework of MLF packages can be a challenge due to their small size. Often MLFs will be mounted on relatively small, thin, and dense PCBs that introduce further challenges due to handling and heating issues. Since reflow of adjacent parts is not desirable during rework, the proximity of other parts further complicates rework. Because of these complexities, the following discussion only provides basic guidelines and a starting point for the development of a successful rework process.

The rework process involves the following steps:

- Component Removal
- Site Redress
- Solder Paste Application
- Component Placement
- Component Attachment

Additionally, prior to rework PNI strongly recommends the PCB assembly be baked for ≥4 hours at 125° C to remove residual moisture from the assembly.

6.1 Component Removal

The first step in removing a component is to reflow the solder joints attaching the component to the PCB. Ideally the reflow profile for removal is the same as that used for attachment. However, the time above liquidus can be reduced once the reflow is complete.

If possible the PCB should be heated from the underside using convective heaters while hot gas or air should be used on the top side of the component. Used specialized nozzles to direct heating only at the ASIC and to minimize heating of adjacent components. Avoid excessive airflow since this may cause the package to skew. Air velocity of 15 – 20 liters per minute is a good starting point.

Once the joints have reflowed, a vacuum lift-off should engage automatically during the transition from reflow to cool down. Because of the component's small size, the vacuum pressure should be kept below 15 inch of Hg. Keeping the pressure low stops the ASIC from lifting out if all solder joints have not reflowed and thus avoids pad liftoff.

6.2 Site Redress

Once the ASIC is removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and a desoldering braid. The width of the blade should match the maximum width of the footprint, and the blade temperature should be low enough not to cause damage to the PCB. Once the residual solder is removed, the lands should be cleaned with a solvent. Usually the solvent is specific to the paste used in the original assembly, so the paste manufacturer's recommendations should be followed.

6.3 Solder Paste Printing

Because of the MLF's small size and fine pitches, solder paste deposition requires extra care. A uniform and precise deposition can be achieved if a miniature stencil specific to the package is used. Align the stencil aperture with the pads under a magnification of 50x to 100x. Next lower the stencil onto the PCB and deposit the paste with a small metal squeegee blade. Alternatively, the mini-stencil can be used to print paste on the package side. A 125 µm thick stencil with an aperture size and shape matching the package land should be used. No-clean flux should be used, as the small standoff of the MLF does not leave much room for cleaning.

6.4 Component Placement

MLF packages are expected to have superior self-centering ability due to their small mass. The placement process of the MLF should be similar to that of BGAs. Since the leads are on the underside of the package, use a split-beam optical system to align the component on the PCB. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. Again, alignment should be done at a magnification of 50x to 100x. The placement machine should allow for fine adjustments in X and Y and the rotation axes.

6.5 Component Attachment

The reflow profile used during the original attachment should be used to attach the new replacement ASIC. Since the reflow parameters have been optimized, using the same profile eliminates the need for thermocouple feedback and reduces operator dependencies.

7 Disclaimer

This document contains general guidelines that PNI Sensor Corporation received from Amkor, its package vendor. PNI does not make direct recommendations for PCB design nor does it take legal liability and responsibility for the information in this document. These guidelines are based

on IPC standard: IPC-SM-782, Surface Mount Design and Land Pattern Standard. This standard has since been superseded by standard IPC-7351B Generic Requirements for Surface Mount Design and Land Pattern Standard. Please refer to the IPC website for more information. See references at the end of this document.

Sketch drawings in this application note are for reference only. They may not represent all MLF applications.

The terms MicroLeadFrame, MLF and the Amkor Technology logo are all registered trademarks of Amkor Technology, Inc.

8 References

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages http://www.amkor.com/go/packaging/document-library
IPC-SM-782 Surface Mount Design and Land Pattern Standard. IPC-7351B Generic Requirements for Surface Mount Design and Land Pattern Standard http://www.ipc.org